

REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Final Office Action of November 10, 2005 (hereinafter "Final Action"). In response, Applicants have amended independent Claims 1 and 12 to clarify that the etch stop layer is formed after the spacers are removed. Applicants respectfully submit that the cited references do not disclose or suggest, at least, the recitations of the pending independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claim 1 is Patentable

Independent Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 6,153,455 to Ling et al. (hereinafter "Ling"). Independent Claim 1 is directed to a method of forming a semiconductor device and recites, in part:

...
forming spacers on sidewalls of the gate pattern, the spacers having a bottom width;
implanting impurity ions using the gate pattern and the spacer as a mask to form a heavily doped impurity diffusion layer in the substrate;
removing the spacers; and
forming a conformal etch stop layer on the gate pattern and the substrate after removing the spacers, wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacers.

Thus, according to independent Claim 1, spacers are formed on sidewalls of the gate pattern and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and *then* an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

Ling describes a method of fabricating a transistor in which a combination of the undoped oxide layer 113 and nitride spacers 134* form sidewalls spacers that are used as masks during ion implantation as shown in FIGS. 5 and 6. In sharp contrast to the recitations of independent Claim 1, however, the undoped oxide layer 113, which is alleged to

correspond to the etch stop layer, is formed before the nitride spacers 134* are removed.
(Ling, FIG. 2--oxide layer 113 formed before spacers 134* are even formed in FIG. 4).

Independent Claim 1 also stands rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,451,704 to Pradeep et al. (hereinafter "Pradeep"). The Final Action alleges that the oxide layer 32 shown in FIG. 4 of Pradeep corresponds to the etch stop layer recited in independent Claim 1. (Final Action, page 4). Applicants respectfully disagree that the oxide layer 32 is an etch stop layer. Instead, the oxide layer 32 is etched to form second gate spacers 32 as shown in FIG. 5 using the same etching techniques as were used to form the first gate spacers 24 of FIG. 2. (Pradeep, col. 9, lines 17 - 38). Applicants submit, therefore, that the oxide layer 32 cannot correspond to the etch stop layer recited in Claim 1.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 1 is patentable over Ling and Pradeep, either alone or in combination, and that Claims 2 - 11 are patentable at least per the patentability of independent Claim 1.

Independent Claim 12 is Patentable

Independent Claim 12 stands rejected under 35 U.S.C. §102(e) as being anticipated by Pradeep. Independent Claim 12 is directed to a method of forming a semiconductor device and recites, in part:

...

- forming spacers on sidewalls of the first and second gate patterns, the sidewall spacers having a bottom width;
- forming a heavily doped impurity diffusion layer in the first active region using the first gate pattern and the spacers on the sidewalls of the first gate pattern as a mask;
- removing the spacers; and
- forming a conformal etch stop layer on the first and second gate patterns and the substrate after removing the spacers,

wherein the second gate pattern is formed to cross over the device isolation layer and to reach the first active region, and

wherein the etch stop layer is formed to a thickness of at least the bottom width of the sidewall spacers.

Thus, according to independent Claim 12, spacers are formed on sidewalls of the gate

patterns and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and *then* an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

As discussed above with respect to independent Claim 1, the Final Action alleges that the oxide layer 32 shown in FIG. 4 of Pradeep corresponds to the etch stop layer recited in independent Claim 1. (Final Action, page 5). Applicants respectfully disagree that the oxide layer 32 is an etch stop layer. Instead, the oxide layer 32 is etched to form second gate spacers 32 as shown in FIG. 5 using the same etching techniques as were used to form the first gate spacers 24 of FIG. 2. (Pradeep, col. 9, lines 17 - 38). Applicants submit, therefore, ~~that~~ that the oxide layer 32 cannot correspond to the etch stop layer recited in Claim 12.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 12 is patentable over Pradeep, and that Claims 13 - 21 are patentable at least per the patentability of independent Claim 12.

In re: Koh et al.
Application Serial No.: 10/625,452
Filed: July 23, 2003
Page 10

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



D. Scott Moore
Registration No. 42,011

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on May 9, 2006.



Traci A. Brown